電機資訊學院 2026 作 BRAIN PLUS HAND 實作專題競賽

Monolithic 3D Hetero-Integration Enabled by BEOL MoS_2-nFDFET and Si-pFinFET

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Abstract: In this study, we demonstrate BEOL-compatible fabrication processes for n-type transistor with MoS2. Our MoS2 n-type Fully Depleted FET (nFDFET) demonstrate excellent gate control and high on/off current ratio (109). Furthermore, we realized a hybrid CFET architecture through hetero-integration of MoS2-nFDFET and Si-pFinFET and successively implement basic logic elements e.g., inverter, NAND, and NOR. These findings highlight the advantages of 2D material in advancing next-generation logic circuits and 3D integrated systems.

Characteristics of MoS_2

2D materials with atomic thickness, high mobility and dangling-bond-free surface exhibit advantages and facilitate M3D hetero-integration.
MoS_2 exhibits n-type characteristics and a high direct bandgap of ~1.8 eV.
There are mature growth and transfer techniques for MoS_2.

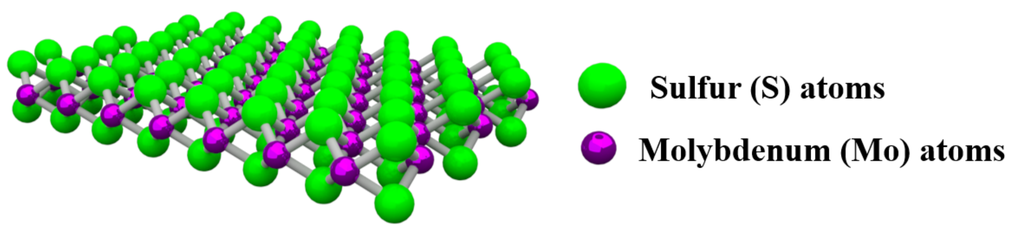

Fig. 1 Structure of MoS_2.

Experiment Process

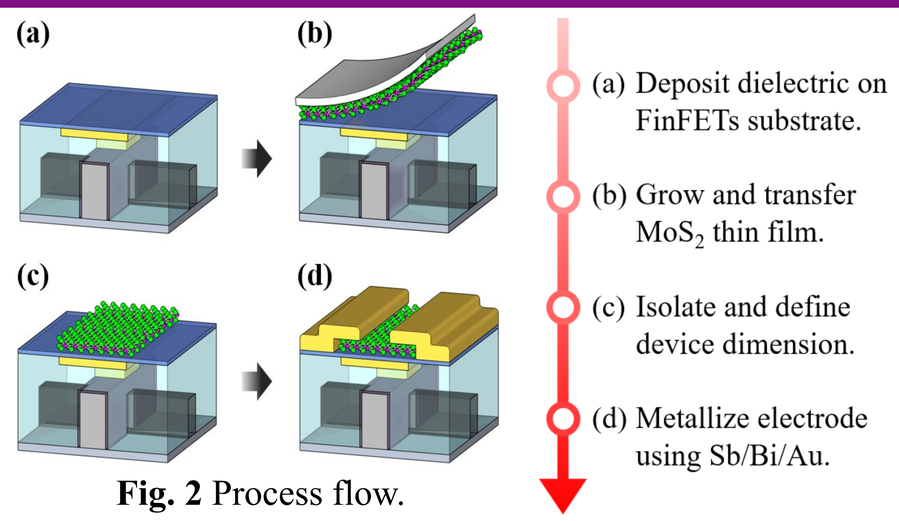

Fig. 2 Process flow.

Experiment Results

1. MoS_2 n-type Fully Depleted FETs

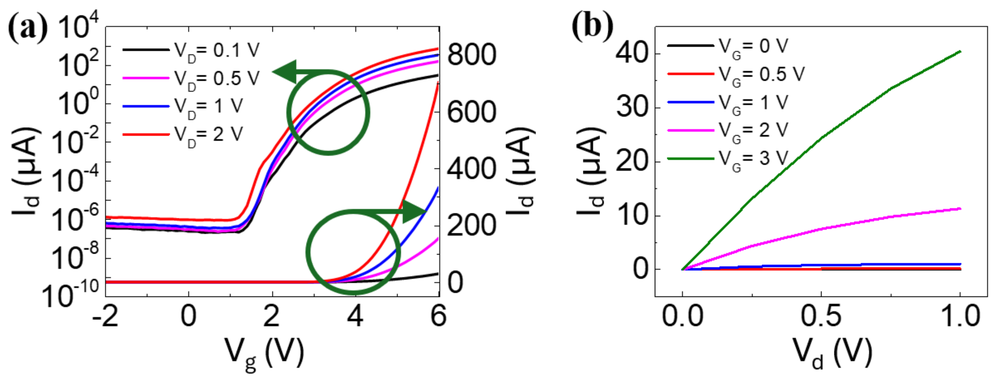

Fig. 3 (a) MoS_2 FDFET I_d-V_g curve. **(b)** MoS_2 FDFET I_d-V_d curve.

Table. 1 Benchmark table for MoS_2 FETs

Ref.	Mobility ($cm^2/V \cdot s$)	On/Off ratio	SS. (mV/decade)
[1]	N/A	1.02×10^5	117
[2]	217	10^8	74
[3]	1.5	2.3×10^6	N/A
[4]	700	10^7	95
[5]	34	2.5×10^6	N/A
[6]	150	10^8	60
This work	17.58	**$> 10^9$**	154

2. Common-Gate CFET structure

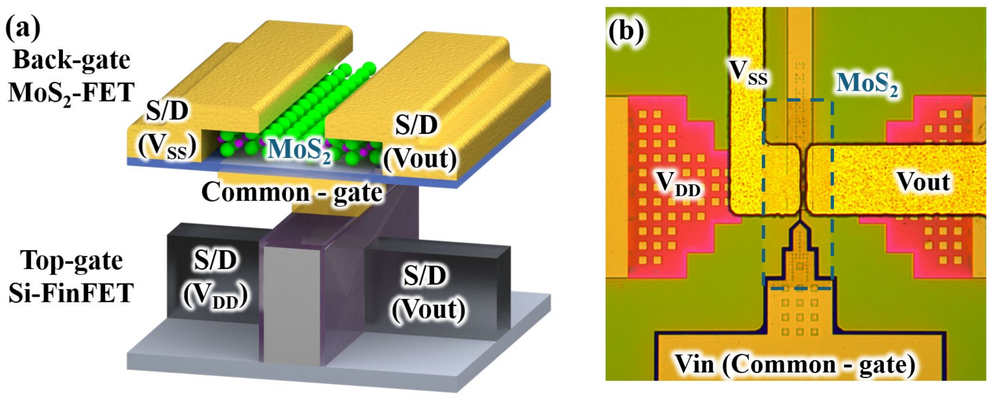

Fig. 4 (a) Common-gate architecture. **(b)** OM image.

Experiment Results

3. INV, NAND and NOR gates

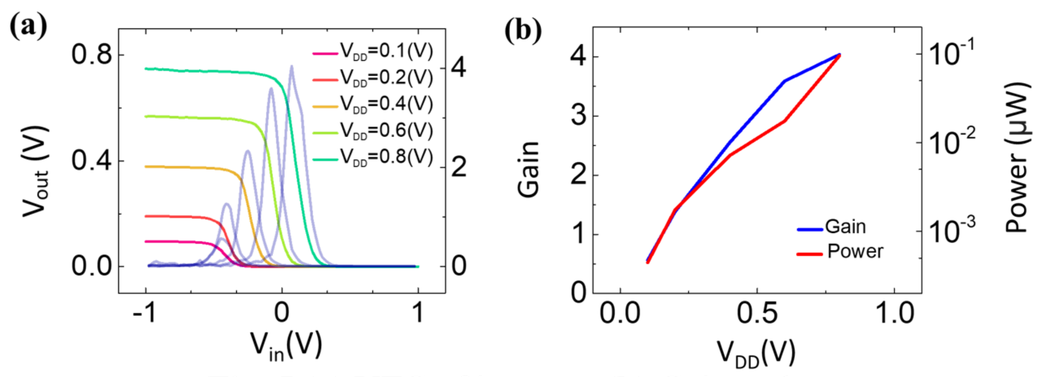

Fig. 5 (a) VTC of inverter. **(b)** Gain and power.

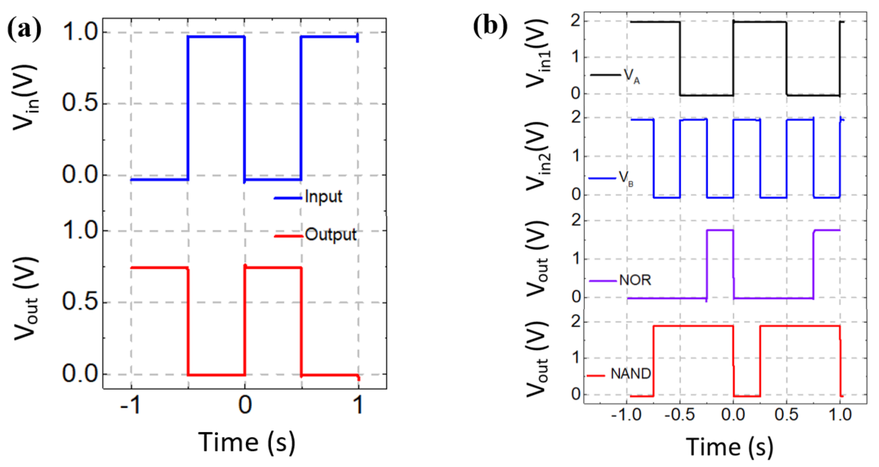

Fig. 6 (a) waveform of inverter. **(b)** waveform of NAND, NOR.

Conclusion

- **High-performance MoS_2 Device**:
  MoS_2-nFDFETs exhibit a high on/off ratio ($>10^9$).
- **Heterogeneous Monolithic 3D Integration**:
  Demonstrate a BEOL compatible process and a M3D hetero-integration of MoS_2 and Si devices.
- **Functional CFET Logic Block**:
  Utilize CFET architecture to implement fundamental logic gates, e.g., INV, NAND and NOR.
- These highlight the advantages of 2D materials with M3D hetero-integration for the next-generation integrated circuit.